IN THE CLAIMS

Please amend the claims as follows:

1. (original) Integrated circuit, comprising:

- at least one processing unit (PU);

- a cache memory (L2_bank) having a plurality of memory modules for caching data;

- remapping means (RM, MapRAM) for performing an unrestricted remapping within said plurality of memory modules.

2. (original) Integrated circuit according to claim 1, wherein said cache memory (L2_BANK) is a set-associative cache.

3. (currently amended) Integrated circuit according to claim 1~~ or 2~~, wherein said remapping means is adapted to perform the remapping on the basis of a programmable permutation function.

4. (currently amended) Integrated circuit according to ~~claims 1 or 2~~claim 1, wherein said remapping means is adapted to perform the remapping on the basis of a reduction mapping.

5. (original) Integrated circuit according to claim 1, further comprising:

a Tag RAM unit (TagRAM) associated to said cache for identifying which data is cached in said cache memory (L2_BANK), and

wherein said remapping means is arranged in series with said Tag RAM unit (TagRAM).

6. (original) Integrated circuit according to claim 1, further comprising:

a Tag RAM unit (TagRAM) associated to said cache for identifying which data is cached in said cache memory (L2_BANK), and

wherein said remapping means is arranged in parallel to said Tag RAM unit (TagRAM).

7. (currently amended) Integrated circuit according to claim 5~~or 6~~, further comprising:

a look up table for marking faulty memory modules.

8. (original) Method of cache remapping in an integrated circuit having at least one processing unit (PU); a main memory (MM) for storing data and a cache memory (L2_BANK) having a plurality of memory modules for caching data, comprising the step of:

performing an unrestricted remapping within said plurality of memory modules.